In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Amended) ~~A~~ An apparatus comprising:

a regulator having an input terminal, a reference terminal and an output terminal, the regulator comprising:

a first amplifier having a first input terminal, a second input terminal and an output terminal, the first input terminal coupled to the reference terminal of the regulator to receive a reference voltage;

a second amplifier having a first terminal, a second terminal and a third terminal, the first terminal coupled to the output terminal of the first amplifier, the second terminal coupled to the input terminal of the regulator to receive an input voltage, the third terminal coupled to the output terminal of the regulator and coupled to the second input terminal of the first amplifier; and

a variable capacitor disposed between the output terminal of the first amplifier and the ~~third~~ first terminal of the second amplifier.

2. (Amended) The apparatus of Claim 1, wherein the variable capacitor comprises a transistor having a first terminal, a second terminal and a third terminal, the first terminal coupled to the output terminal of the first amplifier, and the second terminal and third terminal coupled to the ~~second~~ first terminal of the second amplifier.

3. (Amended) The apparatus of Claim 1, further comprising:

a transistor disposed between the variable capacitor and the third terminal of the second amplifier, the transistor having a first terminal, a second terminal and a third terminal, the first terminal coupled to the ~~second~~ third terminal of the second amplifier, the second terminal coupled to the input terminal of the regulator to receive the input voltage, and the third terminal coupled to variable capacitor; and

a current source coupled to the third terminal of the transistor.

4. (Original) The apparatus of Claim 1, wherein the first amplifier is an error amplifier.

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5. (Original) The apparatus of Claim 1, wherein the second amplifier is a p channel MOSFET transistor.

6. (Amended) The apparatus of Claim 1, further comprising a voltage divider coupled to the ~~second~~ third terminal of the second amplifier and coupled to the ~~third~~ second input terminal of the first amplifier.

7. (Amended) The apparatus of Claim 1, wherein the regulator is a first regulator, the apparatus further comprising a plurality of regulators, each regulator having an input terminal, a reference terminal and an output terminal, wherein the output terminals of the plurality of regulators are coupled together, each of the plurality of regulators comprising:

a first amplifier having a first input terminal, a second input terminal and an output terminal, the first input terminal coupled to the reference terminal of the regulator to receive a reference voltage;

a second amplifier having a first terminal, a second terminal and a third terminal, the first terminal coupled to the output terminal of the first amplifier, the second terminal coupled to the input terminal of the regulator to receive an input voltage, the third terminal coupled to the output terminal of the regulator and coupled to the second input terminal of the first amplifier; and

a variable capacitor disposed between the output terminal of the first amplifier and the ~~third~~ first terminal of the second amplifier;

8. (Original) The apparatus of Claim 7, wherein the apparatus is an integrated circuit, wherein the output terminals of the plurality of regulators are approximately equidistant from a load on the integrated circuit.

9. (Original) The apparatus of Claim 8, wherein the integrated circuit is a programmable circuit and wherein the load has a load resistance and a load current that is dependent on the programming of the programmable circuit.

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10. (Original) The apparatus of Claim 9, wherein the integrated circuit is a field programmable gate array.

11. (Original) A method of regulating a voltage, the method comprising:

providing an input voltage;

providing a reference voltage;

generating a first stage output voltage based on the reference voltage and a feedback voltage;

controlling the amplification of input voltage based on the first stage output voltage to produce a regulated output voltage; and

compensating for instabilities in the input voltage using a variable capacitance between the first stage output voltage and a second voltage based on the regulated output voltage.

12. (Original) The method of Claim 11, wherein the second voltage is the regulated output voltage minus a gate source voltage of a transistor.

13. (Original) The method of Claim 11, further comprising dividing the regulated output voltage to produce the feedback voltage.

14. (Original) The method of Claim 11, further comprising:

producing a plurality of regulated output voltages;

combining the plurality of regulated output voltages;

providing the combined plurality of regulated output voltages to a load.

15. (Original) An integrated circuit comprising:

a plurality of regulators for receiving in input voltage and providing a plurality of regulated output voltages; and

a programmable portion of the integrated circuit, wherein each of the plurality of regulators is approximately equidistant from the programmable portion of the integrated circuit.

16. (Original) The integrated circuit of Claim 15, wherein the integrated circuit is a field programmable gate array.

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17. (Original) The integrated circuit of Claim 15, wherein each of the plurality of regulators comprises a variable capacitor for compensating for instabilities in the input voltage.

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